System Design Collaboration between Frontend & Backend

cooperation with IEC 63055 / IEEE 2401

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SYSTEMC™ EVOLUTION DAY
OCT 23, 2018 | MUNICH | GERMANY

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Contents

- Introduction
- IEC 63055/ IEEE 2401 Concept
- IEC 63055/ IEEE 2401 Future & Collaboration
- Conclusion

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- IEC 63055/ IEEE 2401 Concept
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Background

- Need Seamless Data Transformation among LSI, Package and Board
  - Conversion is needed from one to another
  - Mistakes may occur in manual operation
  - Long verification time even for correct setup

- Time is Money!!
  - Engineers need spend time for innovation
  - Early production gets market share
  - Simpler operation makes better quality

Standardization Strategy

- Make Abstraction Level Higher
- Make Business More Successful
- Make Cost Smaller
- Make Design More Effective
- Make Ecosystem More Attractive

JEITA Semiconductor Organization

Japan Electricals and Information Technology Industries Association

Semiconductor Industry Association in Japan

Semiconductor Standardization Committee in Japan

Semiconductor & System Design Technical Committee

Chair : Yoshinori Fukuba (IEEE P2401 chair / IEC SC47A secretary)

International Standard & Steering Working Group

Leader : Genichi Tanaka (IEEE P2401 Secretary/ TC91WG13 co-convenor)

LPB(LSI Package board) interoperable design sub-committee

Leader: Yoshinori Fukuba

LPB Design Data Exchange Format Working Group

LPB Modeling Working Group

Contents

- Introduction
- Current IEC 63055/ IEEE 2401
- Future IEC 63055/ IEEE 2401 & Collaboration
- Conclusion

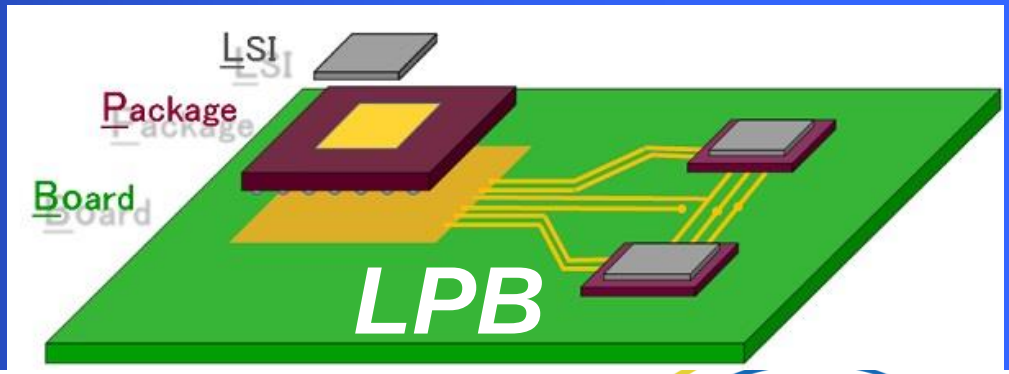
LSI Package Board needs…

- Mutual Communication
- Design Consistency
- Shorten Development Time

Enabled by

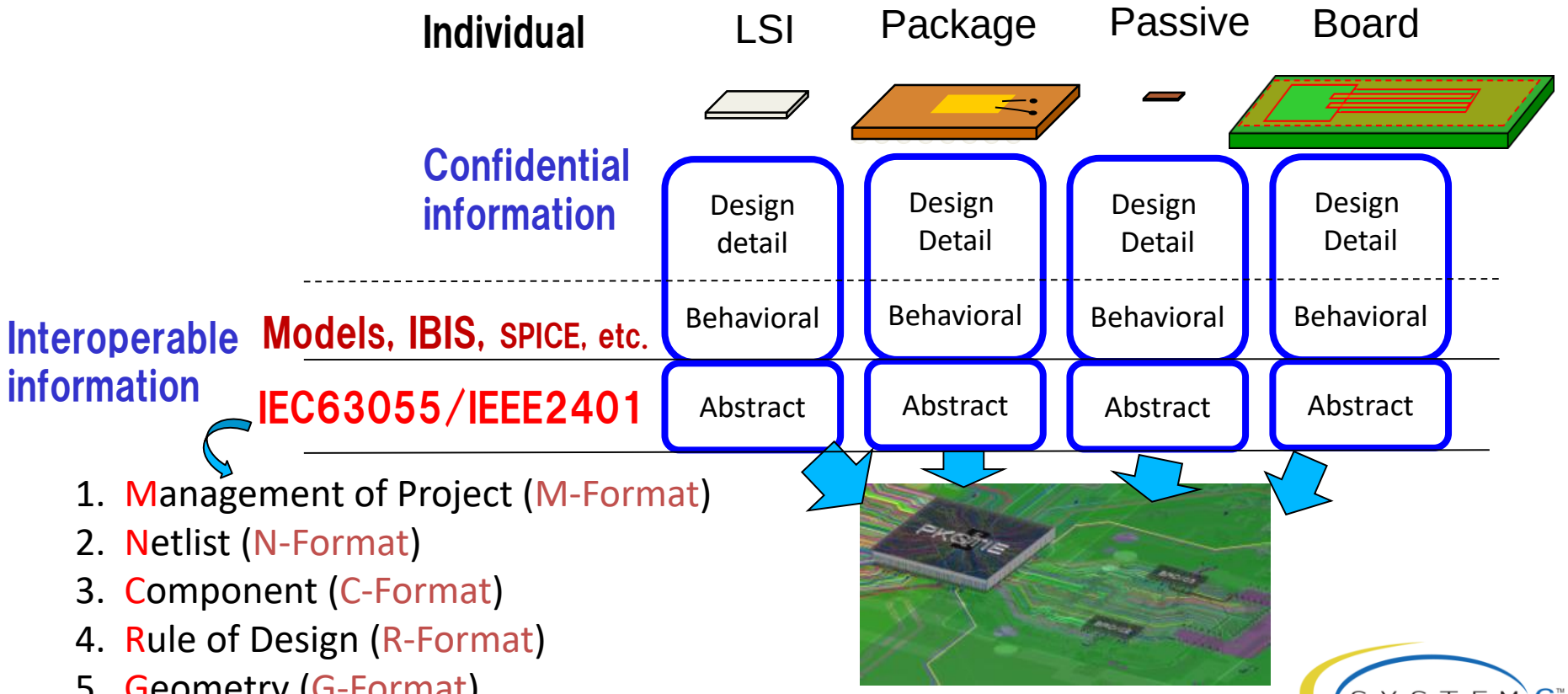
LPB ***Standard formats IEC 63055***

IEEE 2401(dual logo)



What is IEC 63055/ IEEE 2401-2015?

- Standard Format for LSI Package Board (LPB) Interoperable Design.
- For effective information exchange in supply chain.



1. Management of Project (M-Format)
2. Netlist (N-Format)
3. Component (C-Format)
4. Rule of Design (R-Format)
5. Geometry (G-Format)

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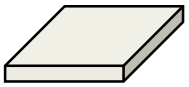
What is IEC 63055/ IEEE 2401-2015?

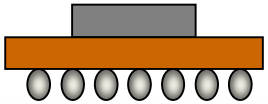
- In the deployment of electronic products…



C-Format

Die Size
Pad location
Spice Model
correspondence

Die models
IBIS/SPICE
CPM/LPM



C-Format

Package size
Terminal location
Spice/IBIS/S-para model
correspondence

Package models
IBIS
S-para SPICE

C-Format

Die mount
Coordinate,
Orientation
Flip, etc.

C-Format

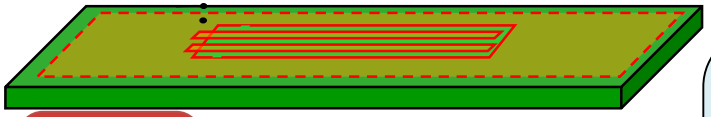
Package mount
Coordinate,
Orientation
Flip, etc.

G-Format **R-Format**

Package Layout
Wire Bonding
Layer stuck-up
Via, material

M-Format

Combination of C, G, R, N which constitute the analysis target



R-Format

Line/Space
Via pitch/size/hole
Layer Stuck up
Material parameter

G-Format

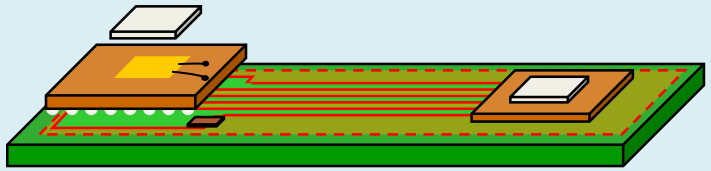
PWB Routing
/Plane

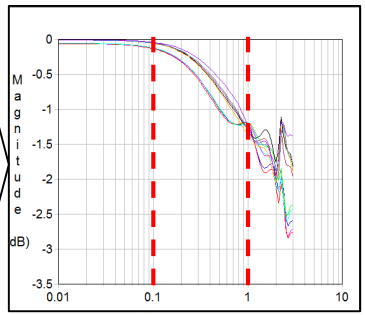
N-Format

Netlist

Connectivity

Simulation Platform





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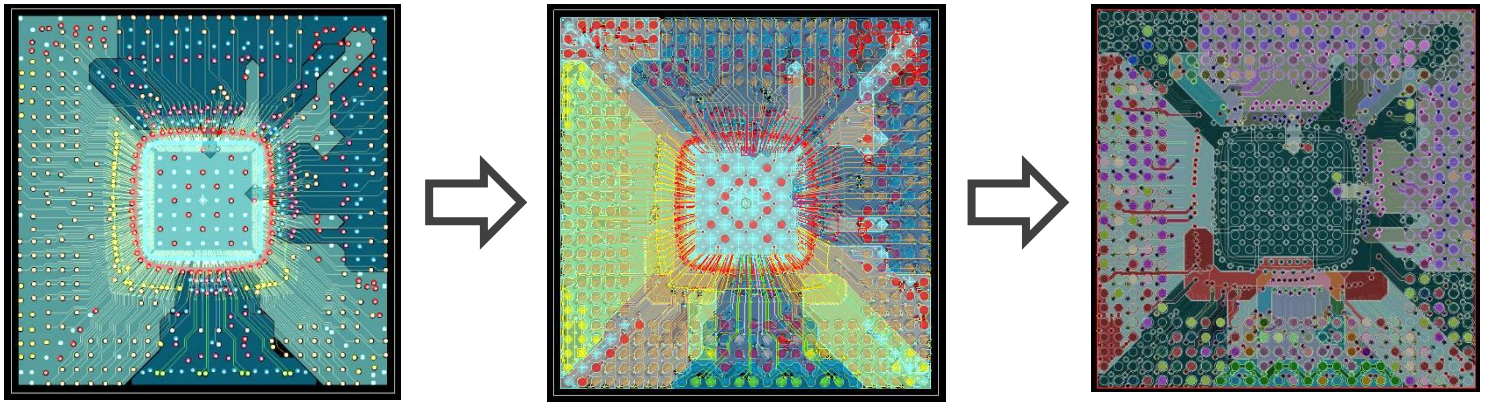
Waste of time – Data conversion

Designers have to use various tools for
LSI tools, PKG tools, Board tools, simulators, CADs, ….

Many data conversions are needed
Format A -> Format B -> Format C
Too complicated to modify data manually for consistency.



Designed by
PKG Planning tool

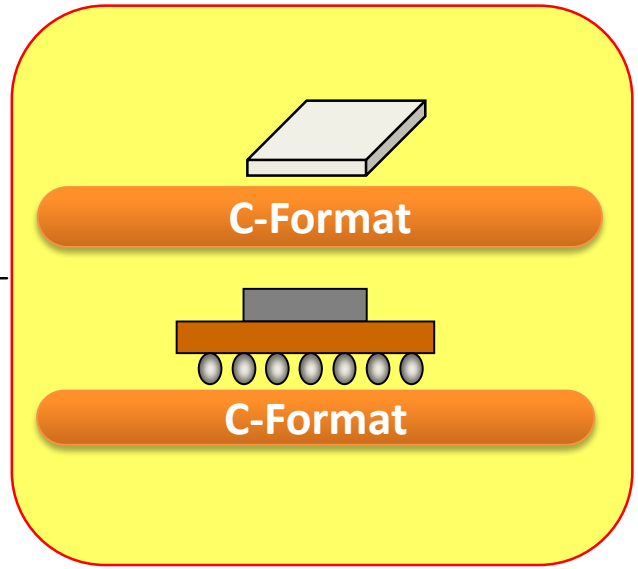
Via
Layout tool data format

Simulation by
EM simulator

Model “ Wrapper”

–■ Function to wrap models to pass models and IPs information to CAD / CAE simultaneously

Geometry
Terminal correspondence
Models
- SPICE
- S parameter
- VHDL (AMS)
- Verilog-HDL
- IEC 62433
- IBIS V4, V7, AMI
- SystemC (AMS)
- New standard models



CAE
(SI,PI,EMC, thermal mechanical)

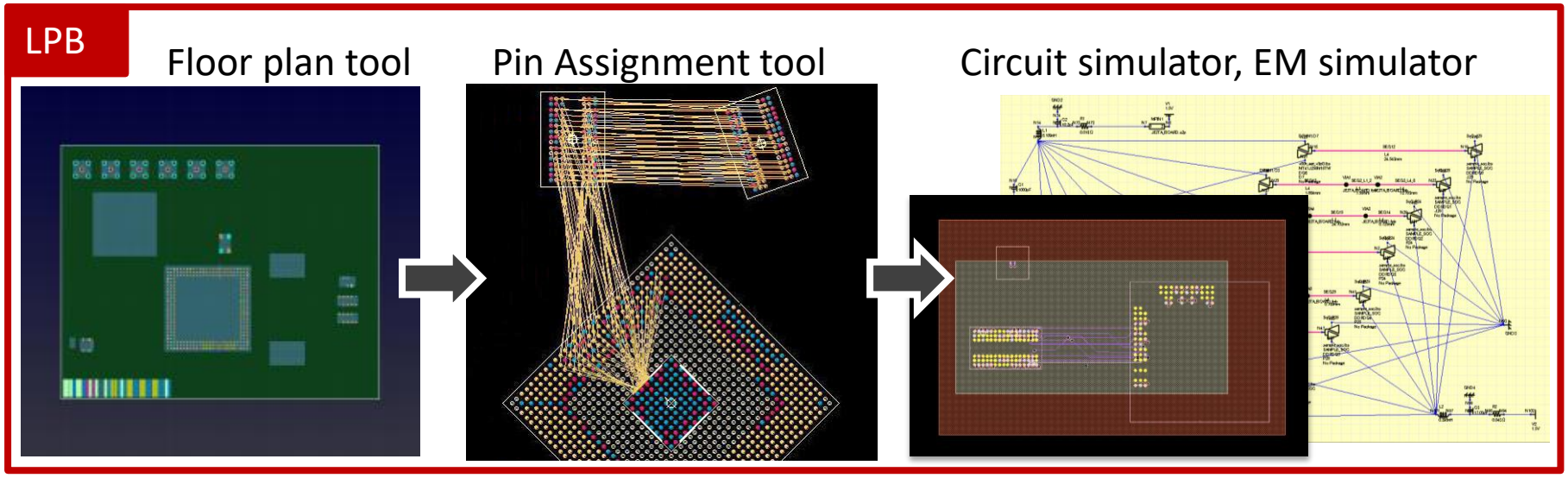
CAD
(Artwork, place, route planning)

LPB Format - Seamless Design

LPB format consists of XML format, and is IEC and IEEE standard.

Various tools support LPB format.

No data conversion is necessary.



LPB has module's physical shape data and layout data.

die outline, PKG outline, die pad shape, PKG ball shape, etc.

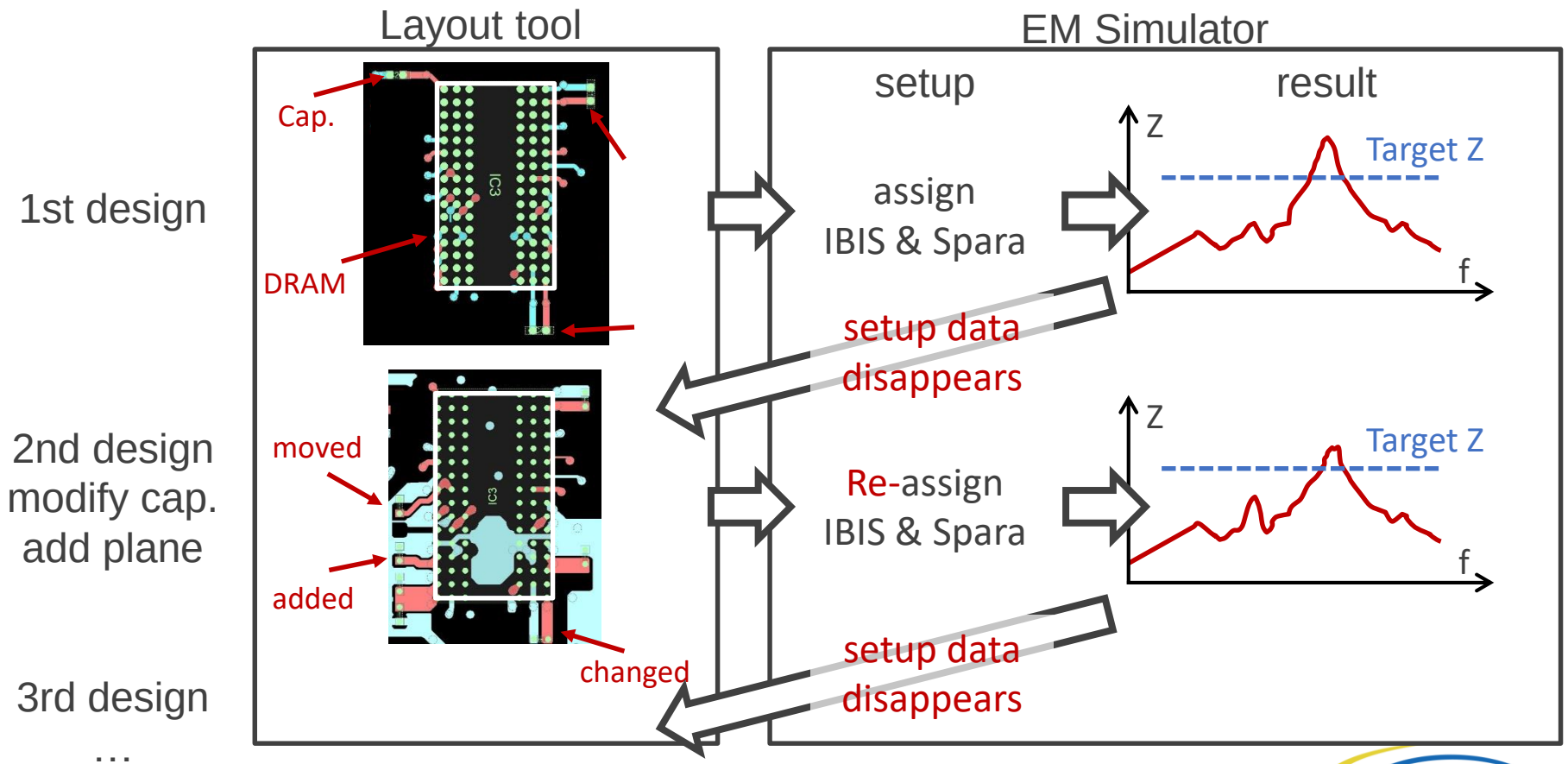
P/G plane shape, transmission line shape, layer stack-up, etc.

In addition, these modules are linked to IBIS models or other models.

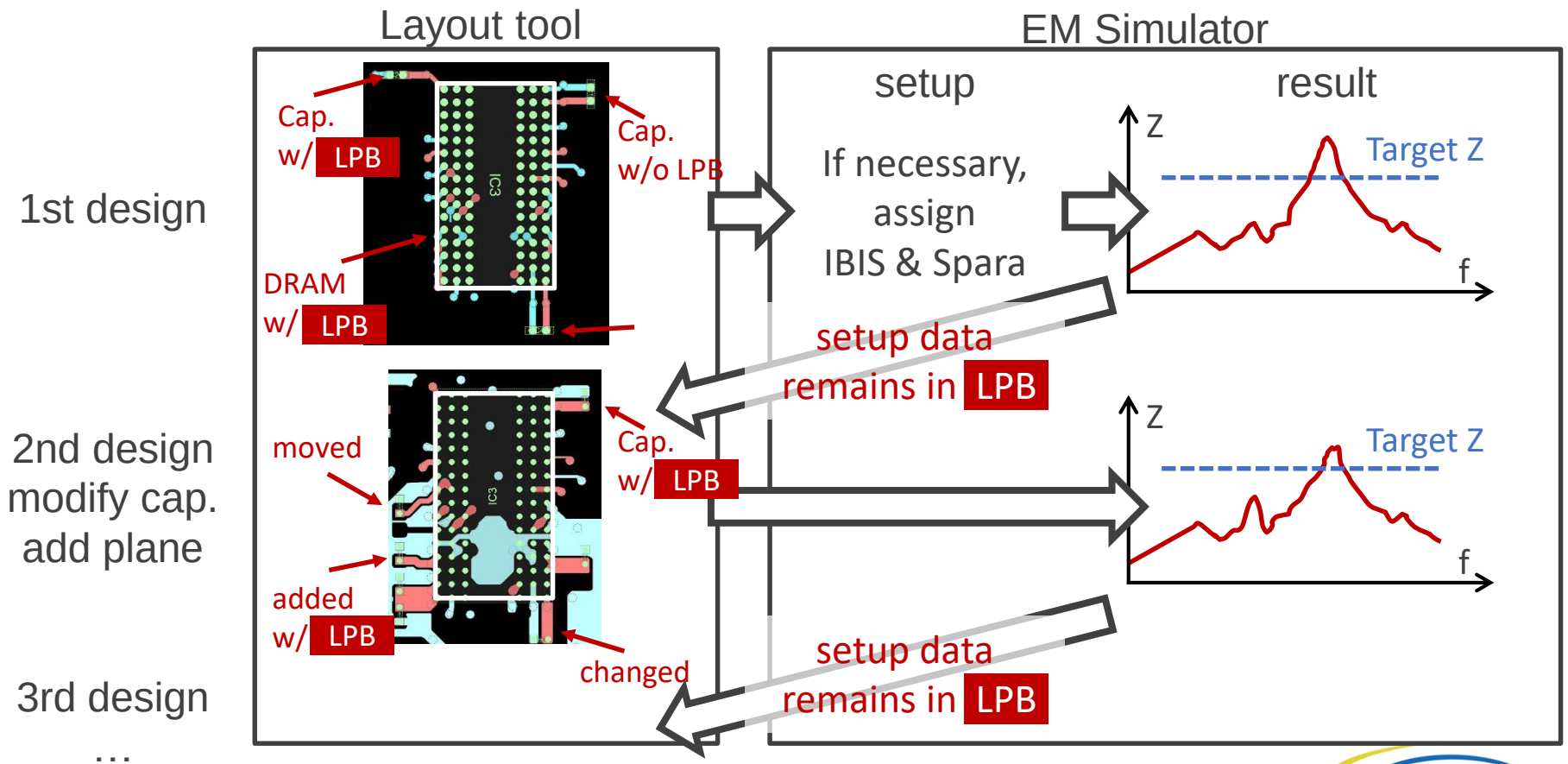
LPB makes it easy to proceed design phase.

Waste of time – Re-setup

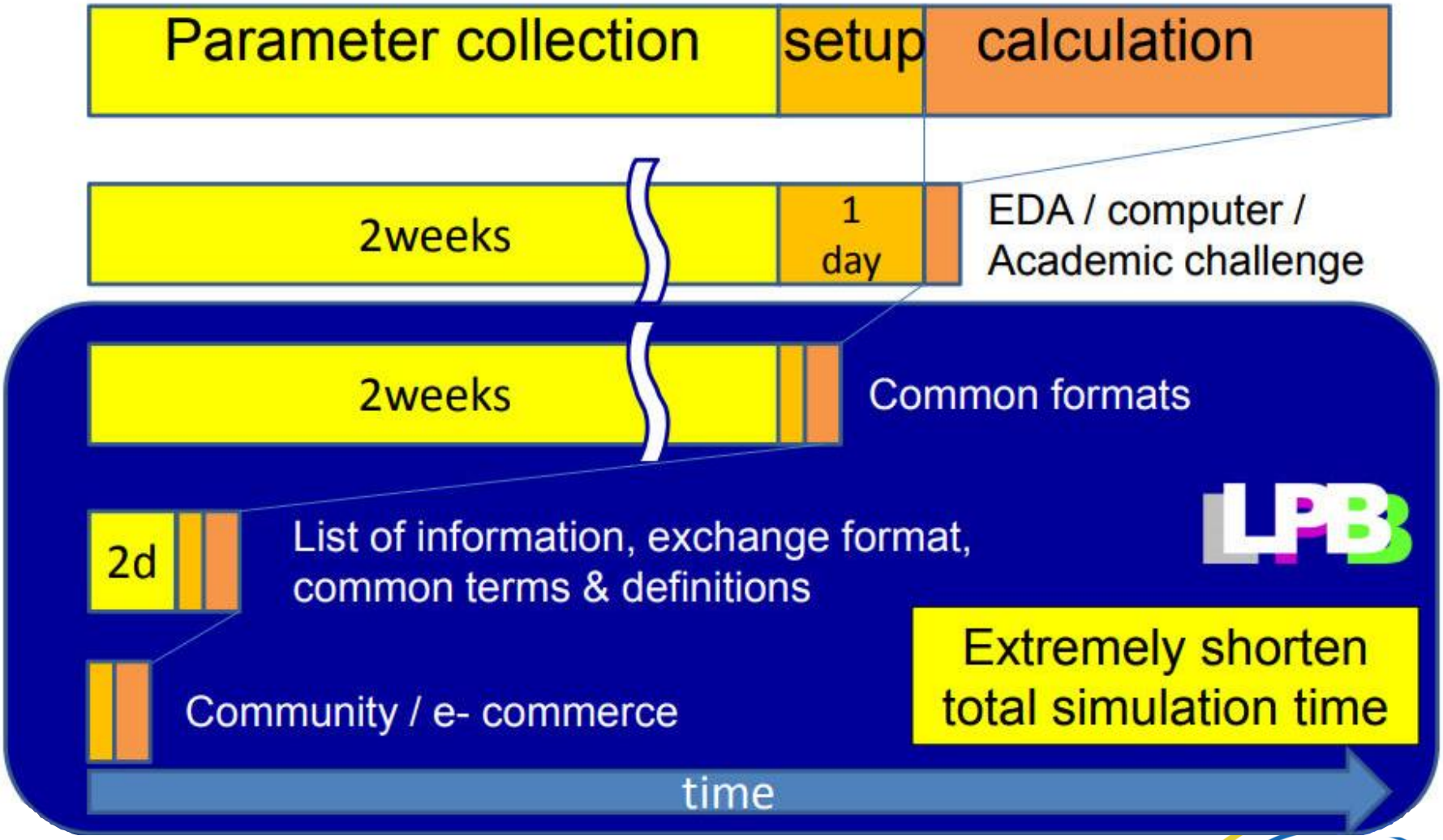
Board layout changes may be occured many times during design phase.
SI/PI/EMC designers also have to do simulation many times.



Once you setup simulation by using LPB, you can reuse it without re-setup.



Effect of IEC 63055/IEEE 2401



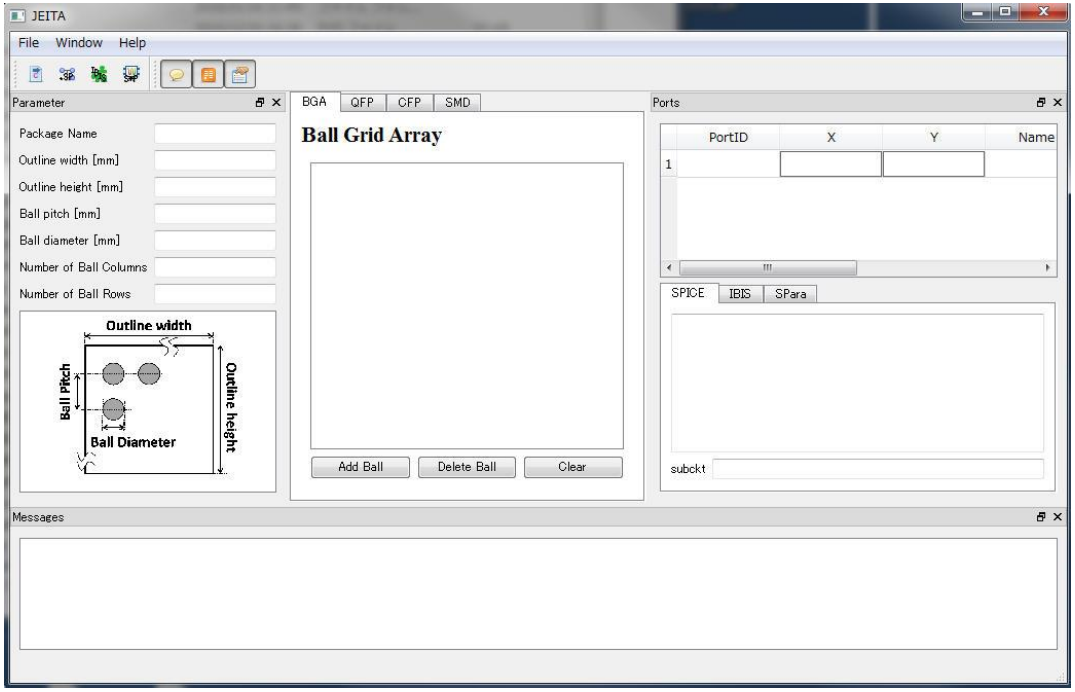
Who provides LPB?

For the components, LPB files should be released by component vendors.

Some commodity parts are getting ready!

JEITA has released the sample data and tools for either vendor or user to create LPB files.

In case you have to make LPB by yourself, use 'LPB design kit' released by JEITA that can export simple LPB files.



http://www.lpb-forum.com/lpb-open-source-project/download/

Sorry, this web site is Japanese.

Contents

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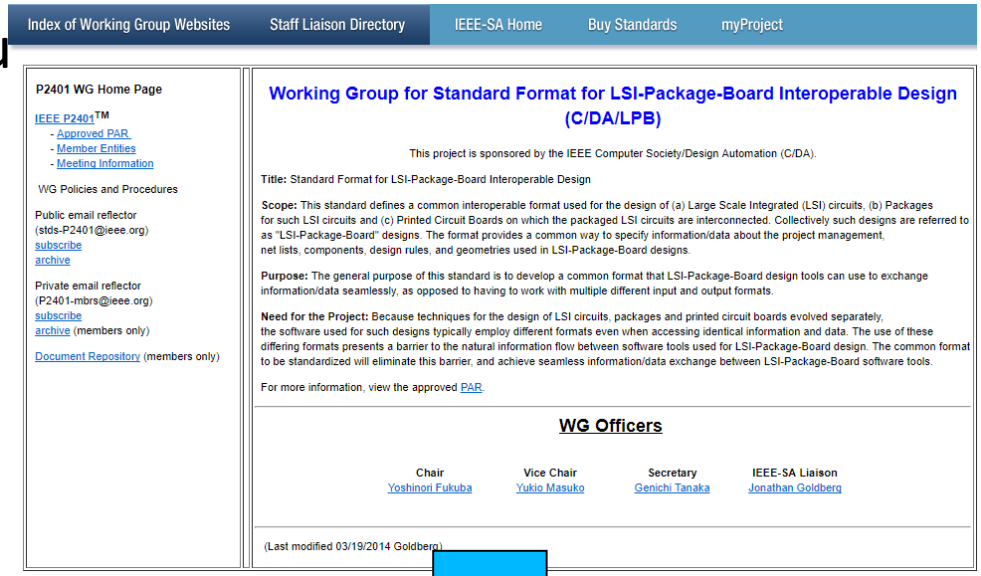
Reference IEEE P2401

- Current Ver.: IEEE 2401-2015
- http://grou



Dual Logo: IEC 63055/ IEEE 2401-2015

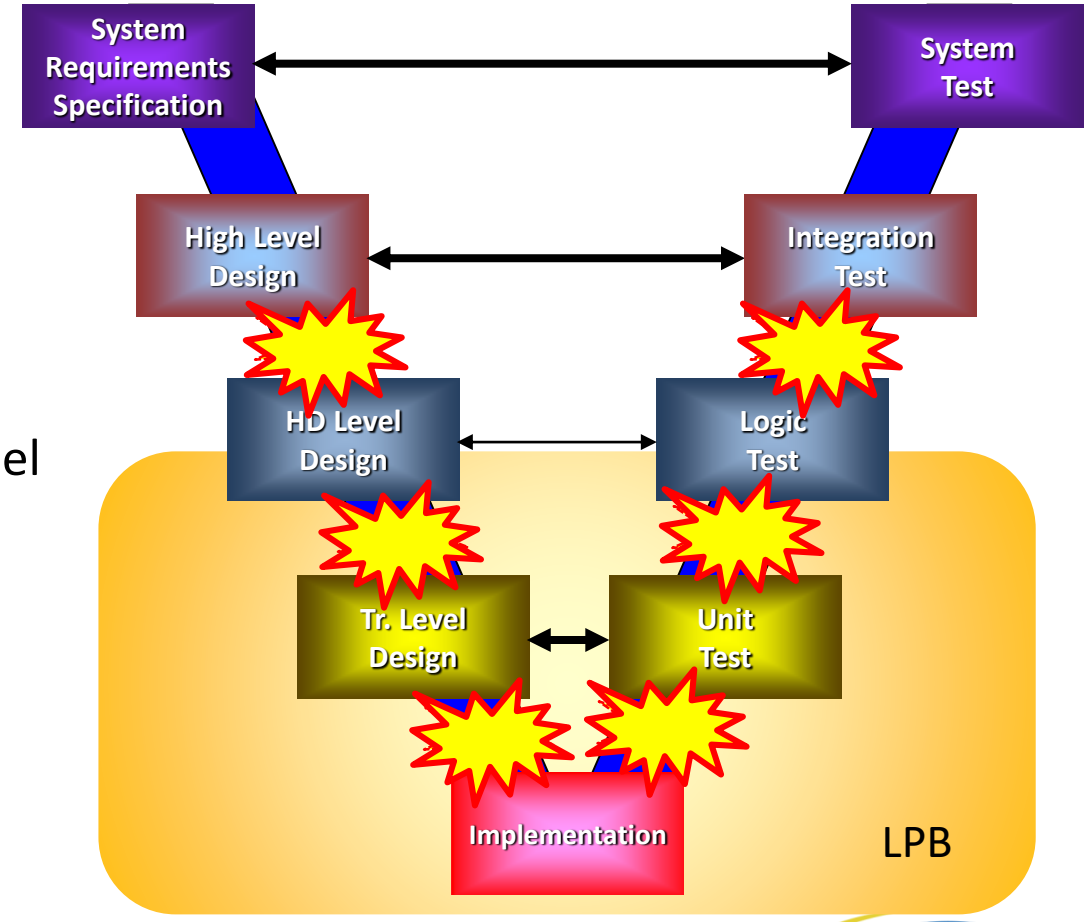
Next Ver.: Target IEEE 2401-2020

System Design

- V-Model
  Ideal: Should work
  Real: Gaps exist

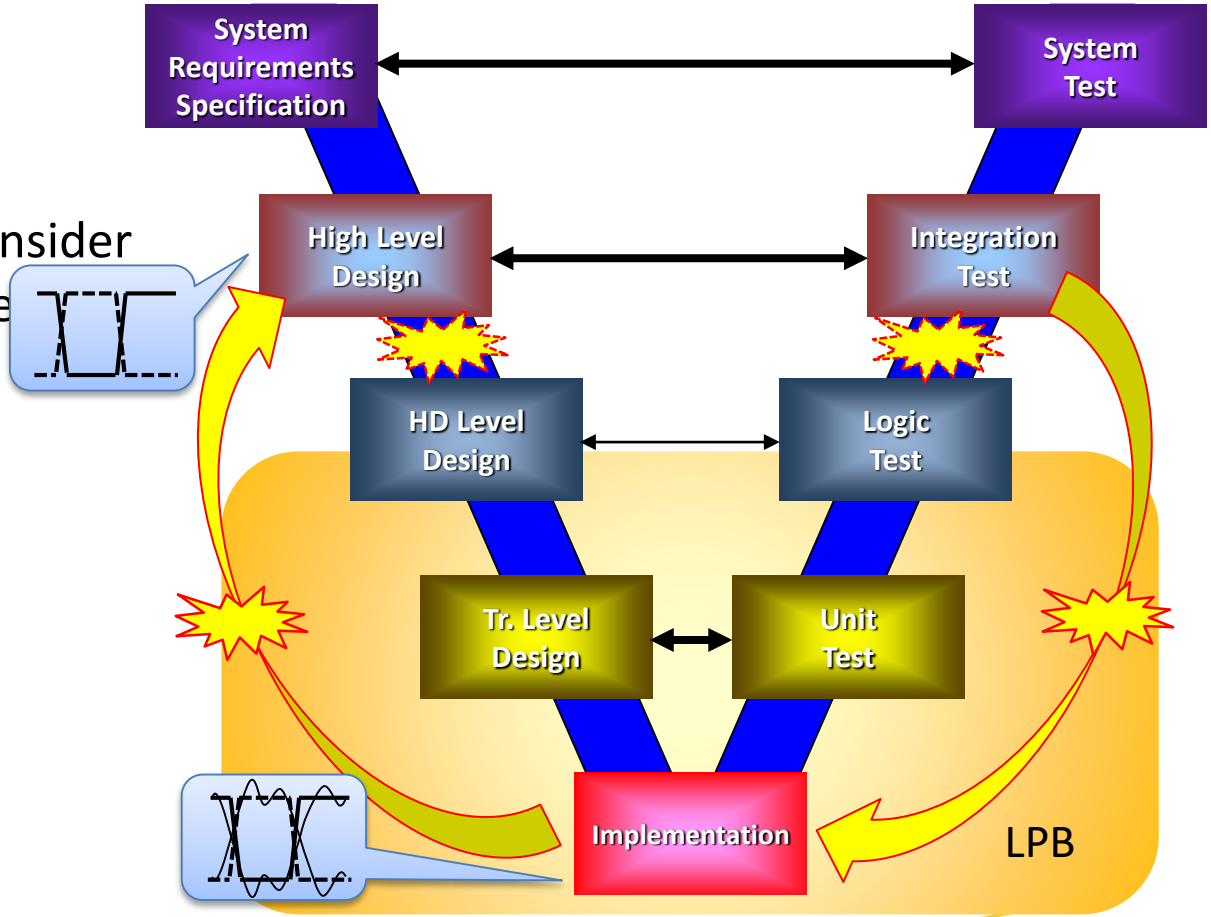
- Design/Verification
  Languages/Tools tackle
- ex.
  High Level Abstraction Model
  High Level Synthesis
  Formal Verification
- LPB format (IEEE 2401)

- Little Digital Issue
  but Analog Ones



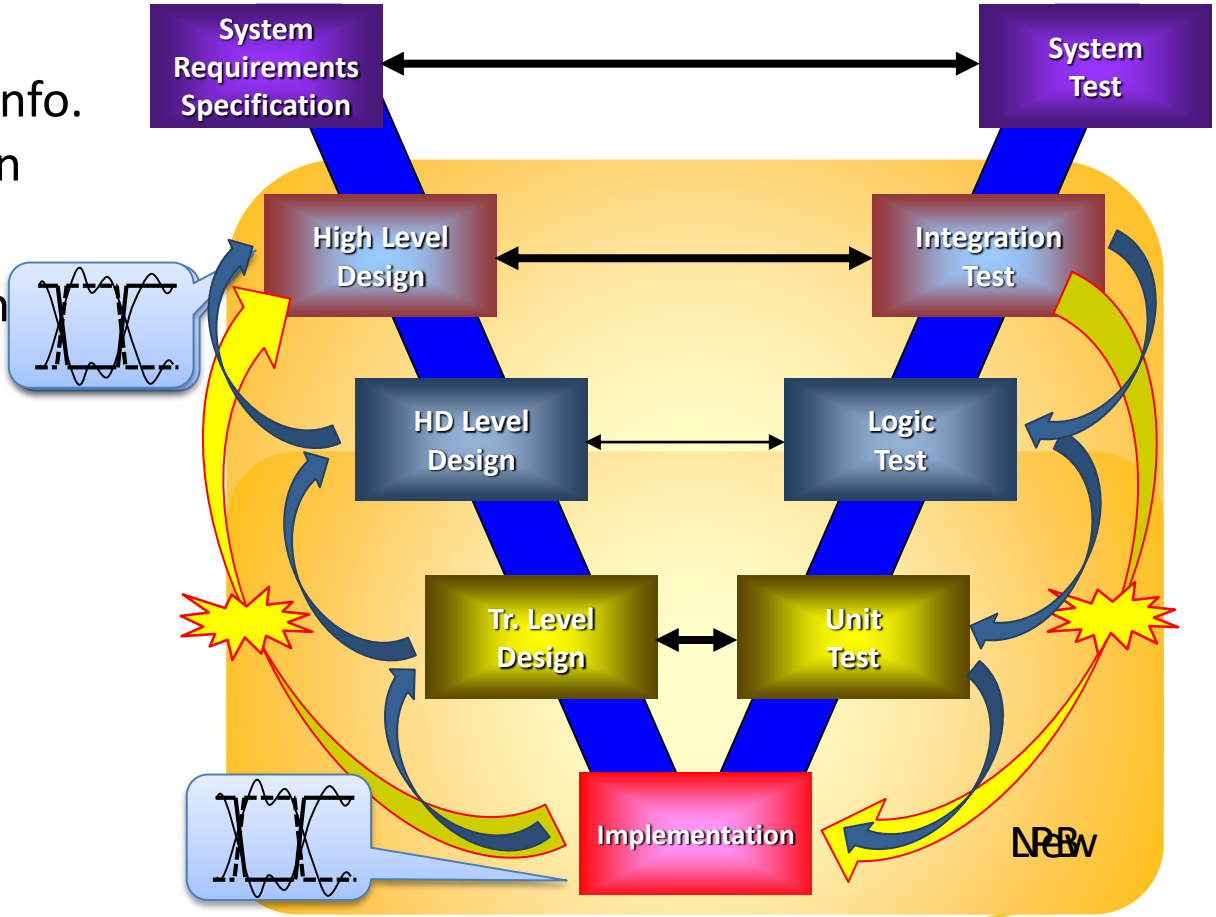
System Design

- Analog Issues
- - Found at final stage
- Because
  Current HLD could consider
  little analog phenome
  - Overshoot
  - Undershoot
  - Eye Opening
  - Jitter
  - Vdrop
  - Thermal
  :



System Design

- Potential Solution
- Library/IP w/Analog Info. for High Level Design
- Common Language which cover differen
- That enables
  Feed Forward Design
  Short TAT
  Margin Less
  High Accuracy
-



Future Plan

- Extension to
  - System Level: Especially Analog Handling
  - Support for More Models
  - Increase of Ease of Use

- Need Consistency for Other Standards
  - Need YOUR System Level Knowledge

Join Our Projects!!

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Conclusion

- Share IEC63055 / IEEE 2401 Concept
  - Mutual Communication
  - Design Consistency
  - Shorten Development Time

- Introduce and Propose Future Plan
  - Schedule IEEE 2401-2020
  - Expansion to System Level and Analog

Join Us to Make Designers Happy!!

Tell us your thought and ideas!!
Let us have offsite meetings at DVCon.

To be on at DVCon on Wed. and on Thu. morning.

Please contact us anytime by skype or email.

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   genichi.tanaka.ur@renesas.com